Monolithic 3D Flash

Andrew J. Walker
Schiltron Corporation

Abstract

The specter of the end of the NAND Flash roadmap has resulted in renewed interest in monolithic 3D approaches that continue the drive to decreasing cost per bit. An abundance of new 3D stackable devices is being pursued by various companies and institutions. This article looks at these different approaches.

The Drive to Innovate

NAND Flash has come a long way since its inception in 1988.[1] Its success has resulted in a race to scale that is faster than CMOS. At the time of writing, manufacturers are working at sub-30 nm half-pitch, also known as 2x nm. Furious activity is taking place to squeeze more electrical bits into each cell, with 4 bits seeming to be the maximum. The cost of this is probably in the area of reliability, with fewer program/erase cycles possible before the smaller threshold voltage windows close.

The problems of NAND scaling [2] have stoked interest in monolithic 3D stacking of Flash cells to keep on the path of reduced cost per bit.[3] “Monolithic” refers to the process where Flash cells are stacked within layers that have been sequentially deposited or grown on top of a wafer in one uninterrupted process run. The wafer itself may contain the driving circuitry for the memory. This distinguishes it from wafer stacking and the use of through silicon vias.

It should be apparent that it is not intuitively obvious what the cost advantage should be, if any, of monolithic 3D compared to the existing 2D approach. The extra processing needed in 3D adds its own cost in two ways; namely, additional step count and potential yield lowering. The positive impact of course is smaller Flash chips and therefore more chips per wafer. The total cost leverage can be mathematically calculated,[4] and shows that the gains in 3D are similar to those that drive manufacturers to go to the next node.

A Plethora of Devices

The first family of potentially stackable approaches involves the use of some kind of resistance switchable material.

A. Phase Change Memory (PCM)

Phase Change Memory (PCM) uses chalcogenides, usually in the form Ge_2-Sb_2-Te_5 (GST).[5] A reversible change from amorphous to (poly)crystalline phases, each with its own resistance, is the basis of the approach. Usually, the reset current needed to reach the high resistance state is several hundred microamps.[6] This is an important consideration for 3D and will be discussed below.

B. Perovskite Memory

Another approach within this family uses some form of perovskite material.[7] A possible mechanism for switching involving the movement of oxygen ions in an applied electric field was recently published.[8]

C. Simple Metal Oxide Memory

The third approach within this family uses simple metal oxides as the switching material.[9] Reset currents needed to attain the high resistance state are being engineered down from at least 100μA to be able to reduce power, increase bandwidth and make them stackable. Common oxides in use are formed from titanium and nickel.

D. Solid-State Electrolyte Memory

The last approach to be dealt with here in the family of switchable resistance is solid-state electrolytes.[10] These involve the making and breaking of a metallic filament within a dielectric material.

In any practical implementation of a resistance switchable memory, a select device for each cell would need to be incorporated. Here we can think of transistors or diodes. In a high-density configuration, the smallest footprint appears to be a vertical diode integrated into each cell. Several approaches to making this diode have been published. For instance, in [11], the diode consisted of NiO as p-type and TiO_2 as n-type. The largest forward diode current density reported was 10^3 A/cm^2, which would work out to about 20nA for a 50nm minimum feature-sized cell. Extensive effort has also been directed to making pillar polysilicon diodes. Such a diode with a diameter close to 150nm can deliver tens to hundreds of microamps at reasonable voltage.[12] The challenge is to make such 3D select devices at low enough temperatures that do not affect the switchable material. In [12], the thermal budget for LPCVD amorphous silicon deposition, typically greater than 450°C, was followed by a rapid thermal anneal at 750°C, which may be prohibitively high for some of the materials mentioned above. In addition, the current carrying capability of the diode has to be such that it can deliver the current to reset the material into the high resistance switch. Both challenges can be met with a 2D implementation since the switchable material can be placed on top of a bulk select device. In other words, it would not experience the process temperature budget of the select device, and the select device would have high current drive. It is precisely in 3D where the challenges arise.

The second family of 3D Flash approaches uses some form of series string of memory transistors. This can then be divided into two types; namely, devices in the horizontal plane and devices in the vertical plane.

E. Floating gate and Charge Trap Flash NAND in Horizontal Plane

A 3D stack of floating gate NAND is the obvious approach here.[13] All other published 3D series string approaches are of the charge trap Flash (CTF) type, where charge is stored in a silicon nitride. Three-dimensional TANOS [14] has been intensively studied. Thin-film transistor (TFT)-based SONOS is also an interesting candidate.[15] The author's company has also published in this area, namely the DG-TFT-SONOS.[16] A cross-section TEM of this approach is given in Figure 1.

This approach solves some fundamental challenges associated with CTF series

strings. These challenges involve the need to turn on devices in a series string to be able to read and program any particular cell. This ends up disturbing the charge state of these passed cells. TANOS is the result of several years of activity trying to solve this problem. In the DG-TFT-SONOS approach, the passing is done without any effect on the charge state of each cell.

F. Charge Trap Flash NAND in Vertical Plane

Building CTF NAND strings vertically would be greatly beneficial in cost since the number of critical lithography steps would be reduced significantly. The BiCS [17] and the VRAT [18] approaches are interesting in this regard. Both approaches consist of series strings of CTF devices, each with a gate all around structure.

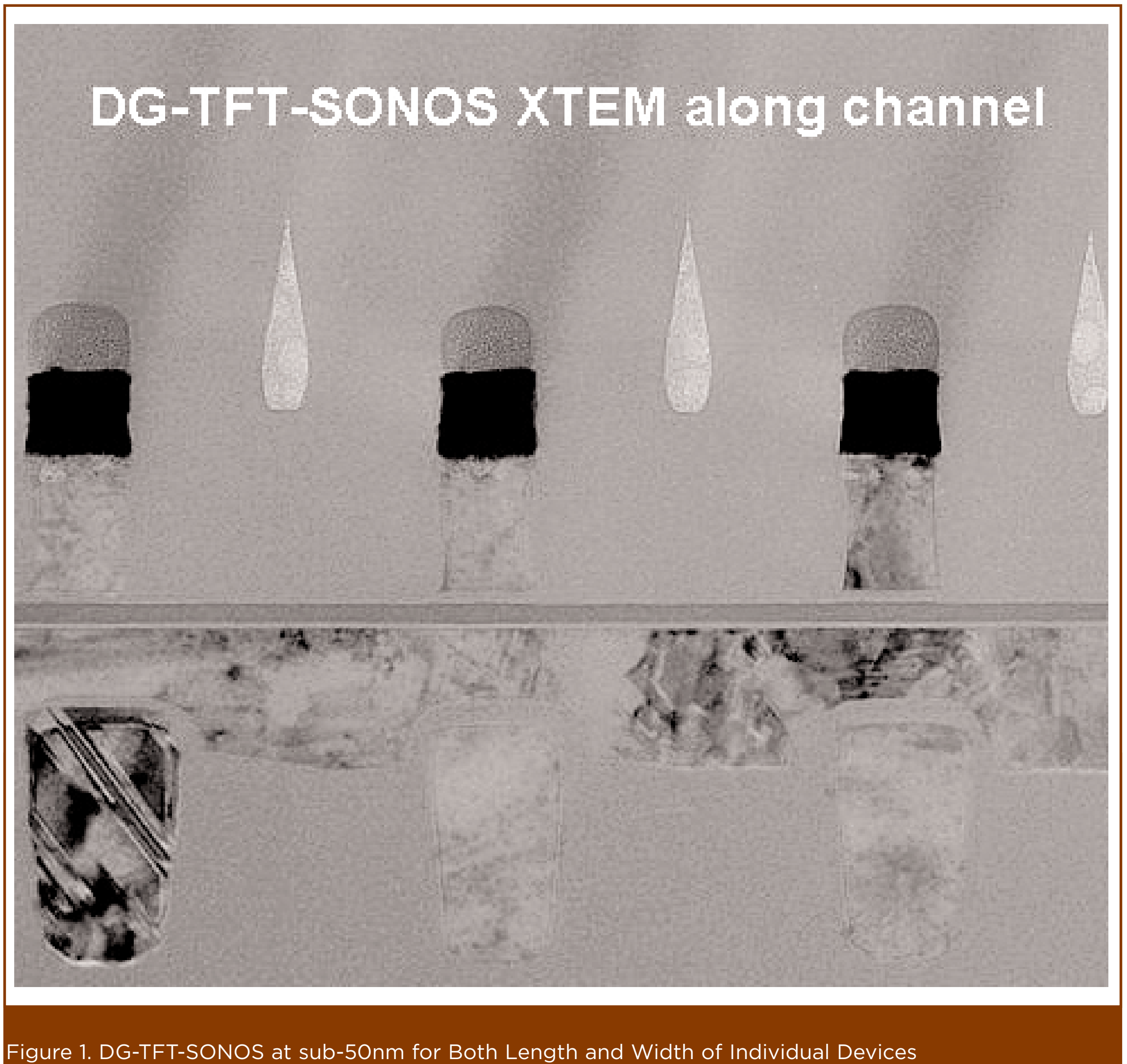

Figure 1. DG-TFT-SONOS at sub-50nm for Both Length and Width of Individual Devices

These would also have to deal with the same challenges that most of the horizontal CTF strings confront; namely, disturbs when passing a signal through to the cell being read or programmed.

Conclusions

Clearly the combination of the success of NAND Flash and its pending scaling difficulties has resulted in feverish innovative activity. The next few years should be very interesting to see which 3D technology or technologies take over the NAND crown. Of equal interest will be the manner in which this happens.

References

1. M. Momodomi et al. "New Device Technologies for 5V-Only 4Mb EEPROM with NAND Structure Cell," I*nternational Electron Devices Meeting Tech. Dig.* pp. 412-415, December 1988.
2. K. Prall, "Scaling Non-Volatile Memory Below 30nm," *Technical Digest*, pp. 5-10, NVSMW, 2007.
3. C. Petti et al. "Monolithic 3D Integrated Circuits," in *Wafer Level 3D ICs Process Technology*, C.S. Tan, R.J. Gutmann and L.R. Reif (Eds), Spring 2008.
4. A.J. Walker, "A Manufacturing Cost Model for 3-D Monolithic Memory Integrated Circuits," *IEEE Trans. Semicond. Manufacturing*, vol. 22, pp. 268-275, May 2009.
5. S.R. Ovshinsky and H. Fritzsche, "Amorphous Semiconductors for Switching, Memory and Imaging Applications," *IEEE Trans. Elect. Dev.*, vol. 20, pp. 91-105, February 1973.
6. F. Bedeschi et al. "A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage," *IEEE Journal Solid-State Circ.*, vol. 44, pp. 217-227, January 2009.
7. A. Beck et al. "Reproducible switching effect in thin oxide films for memory applications," *Appl. Phys. Lett.*, vol. 77, pp. 139-141, July 2000.
8. R. Meyer et al., "Oxide dual-layer memory element for scalable non-volatile cross-point memory technology," Non-Volatile Memory Technology Symposium, pp. 1-5, November 2008.
9. .G. Baek et al. "Highly Scalable Non-volatile Resistive Memory using Simple Binary Oxide Driven by Asymmetric Unipolar Voltage Pulses," International Electron Devices Meeting Tech. Dig., pp. 587-590, December 2004.
10. M.N. Kozicki et al. "Nanoscale Memory Elements Based on Solid-State Electrolytes," IEEE Trans. Nanotech., vol. 4, pp. 331-338, May 2005.
11. I.G. Baek et al. "Multi-layer Cross-point Binary Oxide Resistive Memory (OxRRAM) for Post-NAND Storage Application," *International Electron Devices Meeting Tech. Dig.*, pp. 750-753, December 2005.
12. S.B. Herner et al. "Polysilicon Memory Switching: Electrothermal-Induced Order," *IEEE Trans. Elect. Dev*., vol. 53, pp. 2320-2327, September 2006.
13. K.-T. Park et al. "A Fully Performance Compatible 45 nm 4-Gigabit Three Dimensional Double-Stacked Multi-Level NAND Flash Memory With Shared Bit-Line Structure," *IEEE Journal Solid-State Circuits*, pp. 208-216, January 2009.
14. S.-M. Jung et al. "Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Layers on ILD and TANOS Structure for Beyond 30nm Node," *International Electron Device Meeting Tech. Dig.*, pp. 1-4, December 2006.

15. E.-K. Lai et al. "A Highly Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory," *Symp. VLSI Tech.*, pp. 46-47, 2006.
16. A.J. Walker, "Sub-50nm DG-TFT-SONOS – The Ideal Flash Memory for Monolithic 3D Integration," *International Electron Devices Meeting Tech. Dig.*, pp. 847-850, December 2008.
17. H. Tanaka et al. "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory," Symp. *VLSI Technology Tech. Dig.*, pp. 14-15, 2007.
18. J. Kim et al. "Novel 3D structure for ultra high density flash memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE)," *Symp. VLSI Tech. Tech. Dig.*, pp. 122-123, June 2008.

About the Author

Andrew Walker

Andrew Walker studied physics in Scotland and obtained his Ph.D. in the Netherlands. He entered the semiconductor industry in 1985 with Philips Research. Dr. Walker has worked in several areas including MOS physics and technology, nonvolatile memories and ESD protection. He is founder and president of Schiltron Corporation in Mountain View, California. ■

Click here to return to Table of Contents

PRINT this article E-MAIL this article