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Solving the Read Disturb and String Currents Challenge with 3-D Dual-Gate Flash

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Abstract

Reading NAND Flash cells while minimizing disturbs and maximizing string currents is becoming of major concern with new techniques very recently being proposed for mitigation. While disturb in unselected strings can be addressed, the selected string remains a problem. These effects are greatly exacerbated in any of the 3-D NAND Flash architectures published to date because of the transition to charge trapping and non-crystalline channels. For the first time, this paper presents the magnitude of these challenges in 3-D NAND Flash. The experimental data linking string currents and disturbs show that only a poor compromise between the two seems attainable. Finally, it is shown how the dual-gate thin-film transistor architecture sidesteps these challenges allowing large worst case string currents at virtually zero read disturbs.

I. Introduction

The growing importance of read disturb in advanced NAND Flash has been reported recently where methods have been developed to reduce its impact in unselected strings [1], [2]. Channel boosting in unselected strings is also being used to maintain worst case string currents (defined as the string current when all passing cells are at the highest programmed threshold voltage) above 100 nA [3].

Since thin-film transistor charge trap flash was first introduced [4], various 3-D NAND Flash architectures have been proposed [5], [6], [7], [8]. Challenges associated with read disturb and worst case string currents are greatly exacerbated in going to a 3-D NAND Flash architecture for two main reasons. First, the use of charge trapping requires much thinner tunnel oxides than in the floating gate approach. Second, non-crystalline channels result in much lower carrier mobilities and string currents. The higher pass voltages needed in 3-D to ameliorate the small string currents then combine with the thin tunnel oxide to produce large disturbs.

The link between simultaneously maximizing worst case string currents and minimizing read disturbs is the pass voltage used for read. No doubt, the techniques described elsewhere can be used in 3-D NAND to alleviate the read disturb in the unselected strings and boost the selected string's worst case string current somewhat [1], [2], [3]. However, the focus then shifts to the read disturb in the selected string and what level of worst case string current should be expected.

These critical read challenges in 3-D NAND have not yet been discussed in the literature. Consequently, for the first time, this paper reports on 3-D experimental string currents as a function of string length and pass voltage along with the read disturbs that arise. Not only can this be used to test the viability of various 3-D NAND approaches,

this study also shows how the dual-gate structure fabricated for this effort can be used to sidestep these challenges by decoupling the maximization of worst case string current from read disturb.

II. Experimental

The nonvolatile dual-gate thin-film transistors (DG-TFT) along with their fabrication details have been described before [9], [10]. Elemental channel width and length are about 75 nm. The gate dielectric ONO stack was formed such that the thicknesses from XTEM were 2.5 nm / 9 nm / 5 nm (with tunnel oxide given first). The structure's utility for this study comes from the fact that, not only can it be used as a dual-gate string, it can also be used to mimic the 3-D NAND Flash string without disturb complicating the results.

Figure 1 shows schematically how the DG-TFT string structure is used to measure the string currents that would be expected in 3-D NAND Flash with non-crystalline channels. Notice the use of the underlying access gated devices. In the case of dual-gate use, these are the link to the memory device being read. In the case of mimicking 3-D NAND Flash, these are used as the only link to the device being read with the read-pass voltage over and above the access devices' threshold voltage equivalent to the NAND string's read-pass voltage over and above the maximum programmed threshold voltage. The threshold voltage of the access device measured as a single element is 2 volts at 10 nA source – drain current. When a read-pass voltage of, for example, 6 volts is applied to the access devices, this then is equivalent to a read-pass overdrive voltage of 4 volts. The current path is from the bitline, through the inversion channels of the access devices, through the memory cell being read and then through the inversion channels of the rest of the access

devices to the source. All unselected memory gates are held at -3 volts to make sure the memory devices do not conduct. The greater the read-pass overdrive voltage is, the lower the resistance is connecting the cell being read to the bitline and the source.

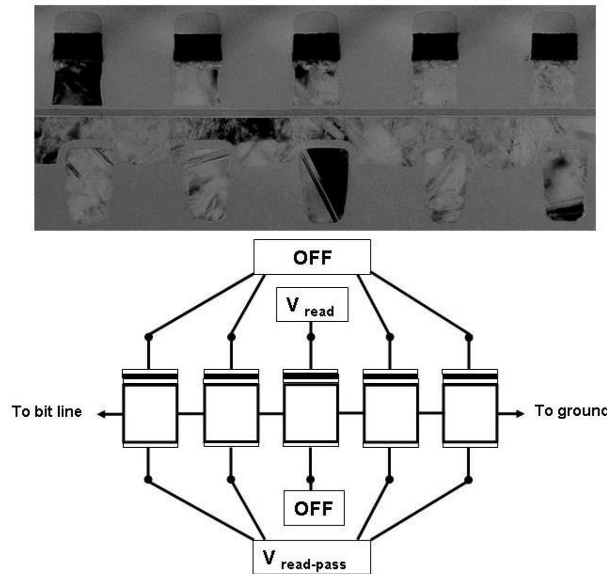

Figure.1: *The dual-gate TFT string configured to measure the equivalent 3-D NAND string currents as a function of read-pass voltage (Vread-pass). The devices held off are done so with -3 volts on their gates. The source is at ground and the bit line is at 0.5 volt. The current path is from the bitline, through the inversion channels of the access devices, through the memory cell being read and then through the inversion channels of the rest of the access devices to the source.*

3-D NAND Flash worst case string current as a function of read-pass overdrive voltage can then be measured. For instance, if a 3-D NAND string has a maximum programmed threshold voltage of 6 volts, then the above approach with 4 volts read-pass voltage, resulting in 2 volts read-pass overdrive voltage, would be equivalent to the 3-D

NAND worst case string current with 8 volts read-pass. Any erased-state low threshold voltage cell in the selected string (we shall assume that unselected strings can be dealt with using the techniques recently reported [1], [2], [3]) will experience this read-pass voltage mitigated to a certain extent by the bitline voltage of around 1 volt. The resultant disturb is measured here on a single device by ignoring the access device and applying the read-pass voltage to the memory gate.

The advantage of using the dual-gate architecture is shown through measurements of string current as a function of read-pass voltage using the access devices. The resultant disturbs are measured as a function of access device read-pass voltage and compared with disturbs in the 3-D NAND Flash case.

III. Results and Discussion

Figure 2 shows the experimental string currents as a function of read-pass overdrive voltage with string length as a parameter. Also included are educated guesses for what would be achieved with longer strings. The algorithm used to generate the latter is simply based on the vertical separation seen each time an actual measured string is doubled in length. This should be fairly accurate given the fact that it is just a series resistance increase.

In any 3-D NAND string with all selected string passing cells in their maximum threshold voltage programmed state, these curves show the expected worst case string currents as a function of read-pass voltage over and above this maximum threshold voltage. The worst case string current multiplication going from 1 volt to 5 volts read-pass overdrive increases from around 5 for the 16 cell string to greater than 30 for strings

of 64 cells and longer and can be explained by the rising dominance of the passing cell resistance with lengthening string.

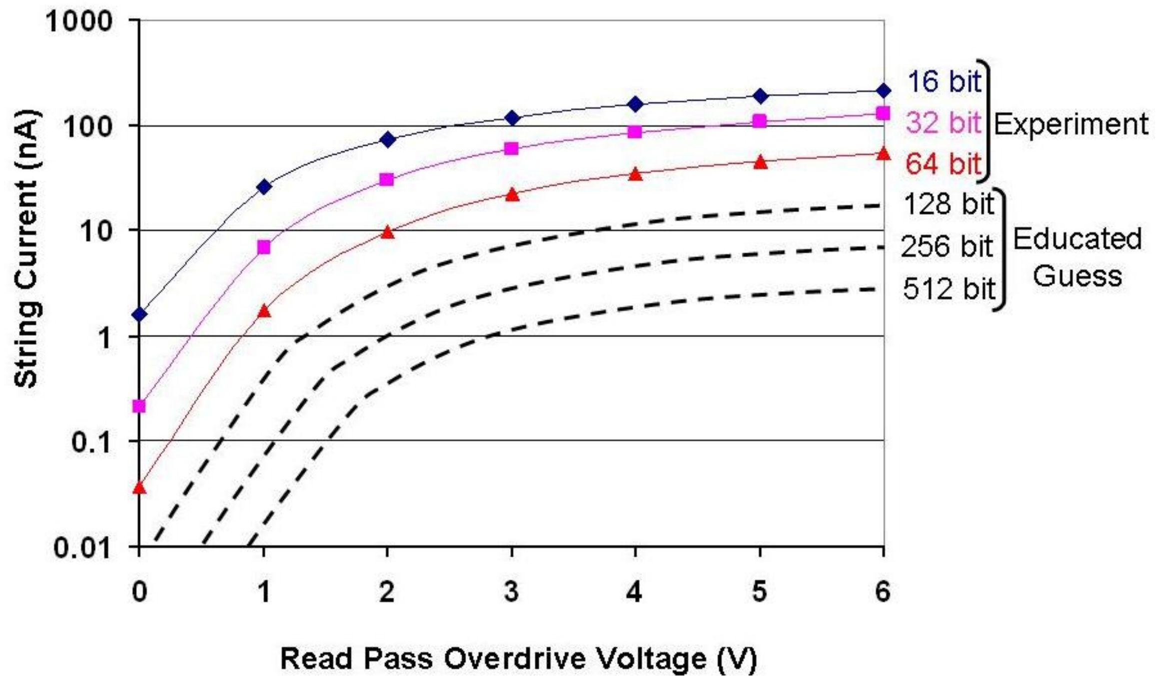

Figure 2*: String currents measured using the conditions in Fig.1. The read-pass overdrive voltage is the access gate voltage over and above the 2 volt access device threshold voltage. Both experimental data and educated guesses are given.*

To avoid worst case string currents vanishing below tens of nA's, clearly the read-pass overdrive voltage should be maximized. The challenge is to do this while controlling disturb in selected string passing cells where the worst case would be the erased state. Figure 3 shows the threshold voltage drift in a single cell starting out in the erased state with the read-pass voltage as the parameter. The programmed state threshold voltage in this particular case is around 5 volts so these read-pass voltages have also been converted to read-pass overdrive voltages to be able to compare with the worst case string currents.

It is clear that even 4 volts read-pass overdrive voltage that is needed to maintain worst case string currents larger than tens of nA's has a significant disturb impact on erased state cells. In fact, about a third of the threshold voltage window has been lost after 1 second of stress.

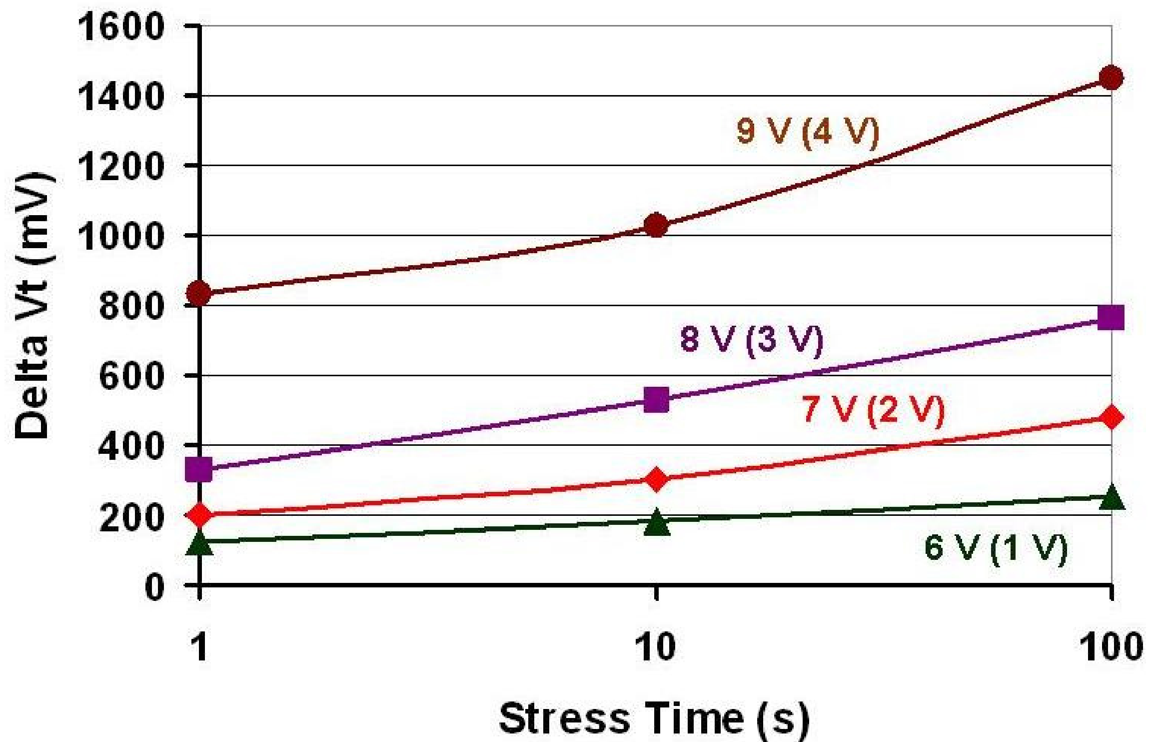

Figure.3*: Single cell threshold voltage evolution with read-pass voltage as parameter when the latter is applied to the memory gate. The device starts out in the erased state for each voltage. The maximum programmed threshold voltage is about 5 volts so the equivalent read-pass overdrive voltages over this are also given in brackets.*

To be able to generalize these results and apply them to existing 3-D NAND Flash architectures where worst case string currents are not usually reported, the following simple algorithm should give good estimates: work out the read-pass overdrive voltage from the read-pass voltage (associated with string currents usually reported in the best

case when all cells are erased) and the maximum programmed threshold voltage; read out the expected worst case string current with this read-pass overdrive voltage and the string length reported using Fig.2; move up the curve in Fig.2 to estimate what read-pass overdrive voltage would be needed to achieve tens of nA's; with this new read-pass overdrive voltage, use Fig.3 to estimate the read disturb characteristics with time. Obviously, low string currents and large disturbs can be mitigated to a certain extent by the level of channel crystallinity and the memory gate dielectric stack thickness respectively but this algorithm should remain a good rule-of-thumb to estimate 3-D NAND Flash worst case string currents and associated read disturbs.

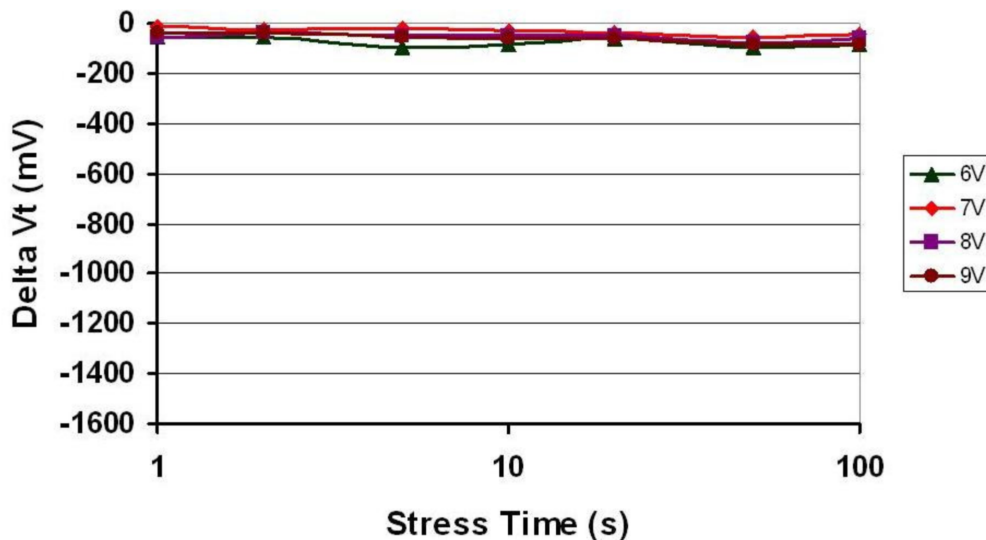

Figure 4*: Single cell threshold voltage evolution when the access gated device is used as the read-pass cell. The device starts out in the programmed state for each access gate voltage. The programmed state threshold voltage is about 5 volts.*

When the access gated device is used as the read-pass cell, the programmed threshold voltage case needs to be monitored for disturb. Figure 4 shows that the stored charge is virtually unaffected by this even with 9 volts applied to the access gate. This is equivalent

to 7 volts read-pass overdrive (over and above the 2 volts access gate threshold voltage). Figure 2 shows that this allows orders of magnitude more current compared to 3-D NAND Flash at the longer string lengths and without read disturb.

IV. Conclusions

For the first time, this paper has shown the interaction between read disturb and worst case string current maximization in 3-D NAND Flash. Large disturbs are inevitable when using read-pass voltage to minimize string series resistance. The advantage of the dual-gate architecture is obvious in that it decouples the string current maximization from the read disturb.

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