3-D NAND Flash Strings, Non-Crystalline Channels, Surface Potentials and Vanishing String Currents

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Abstract

3-D versions of NAND Flash strings are being seen as potential replacements for the classic 2-D approach. Many rely on the use of non-crystalline channel silicon. This paper looks at the consequences of using such a channel in a NAND series string of devices from the viewpoint of each device's surface potential. It is shown that the sluggish response of the surface potential with gate voltage has serious consequences for the level of the string current during read. This poor response exacerbates an already difficult challenge of controlling disturbs in any Charge Trap NAND Flash string. Vanishing string currents as strings lengthen cast doubt on the viability of some 3-D NAND approaches.

I. Introduction

Charge Trap Flash (CTF) NAND has appeared as a contender to replace classic 2-D NAND Flash [1], [2], [3], [4], [5], [6], [7], [8], [9]. All these approaches rely on the ability to pass current through memory cells that are part of the string to be able to read the

memory state of the cell being accessed. In this way, they are all very similar to the classic 2-D NAND Flash that has been so successful over the past 20 years [10].

All of the 3-D CTF NAND approaches referenced above incorporate two key differences from classic 2-D NAND: firstly, the replacement of the floating gate with a SONOS-type (Silicon-Oxide-Nitride-Oxide-Silicon) memory dielectric stack; and secondly, the replacement of a monocrystalline channel with some form of polycrystalline material.

The disturb challenges of having a SONOS-type NAND string have been published before [11], [12]. During a NAND read operation, the gates of the unselected cells must be biased such that they conduct even if they are in a programmed state. This relatively high voltage causes disturb in erased cells. When a threshold voltage "lifetime" was defined as a 2V shift in the erased state, then it was seen that this lifetime could be reduced by a decade for every 0.4 to 0.5V increase in this "read-pass" voltage [12].

The use of some form of polycrystalline channel material introduces an interesting challenge associated with the disturb sensitivity of NAND SONOS. It is well known that thin-film transistors with polycrystalline channels have small source-drain currents. Therefore, placing many in a NAND series string reduces the string current fairly dramatically compared to standard monocrystalline channel NAND Flash. The worst case is when the memory cell being read is in the erased state while all other memory cells in the same string are in the high threshold voltage programmed state resulting in the highest impedance to the cell being read. The normal degree of freedom of over-driving the gates of the unselected pass cells has two problems associated with it: firstly, it results in increasingly troublesome pass disturbs as explained above; secondly, it has limited ability to increase the worst case string current compared to the monocrystalline channel case.

This paper explains the "inertia" of the worst case string current with read-pass voltage in the case of 3-D NAND strings where the channels are composed of some form of polycrystalline material.

The paper is arranged as follows: Section II explains the concepts of localized states in the energy band gap of polycrystalline silicon; Section III looks at the effects of such gap states on the surface potential and on energy barriers to electrical conduction in the transistor inversion layer; Section IV applies this knowledge to generic NAND Flash strings of devices with polycrystalline channels; Section V contains the summary and conclusions.

II. Localized States in the Energy Band Gap

The conduction mechanism in a polycrystalline silicon channel of a thin-film transistor (TFT) has been approached from two main directions in the literature. The first views the conduction as taking place due to thermionic emission over grain boundary energy barriers where crystalline defects are localized. The second assumes that the crystalline defects act as if they are more uniformly distributed such that an effective medium approach can be taken where a spatially uniform level of band gap states controls the conduction. For readers interested in this controversy, a summary of the relevant literature at the time was made by the author in a previous paper [13]. Either approach may be taken and applied to 3-D NAND Flash with polycrystalline channels resulting in the same conclusions. This paper takes the second approach mainly because of previous work by the author that showed the experimental absence of some key predictions made by the first approach [13] although reference will also be made to recent work that has taken the first approach [14].

In a disordered semiconductor such as the channel region of a polycrystalline TFT, the disorder results in localized states in the forbidden energy gap. Key experimental work by Hirose et al. showed the electrical similarities between polycrystalline and amorphous silicon in this regard [15].

Figure 1 shows the electronic density of states postulated by Hirose. Notice the tailing states extending from the band edges E_C and E_V to energy levels E_A and E_B respectively. The envelope function also contains deep levels closer to midgap. Hirose postulated that the deep level states originated from defects throughout the deposited film and were dependent on deposition and annealing temperatures and that tailing states came from the grain boundary regions due to their highly disordered structure.

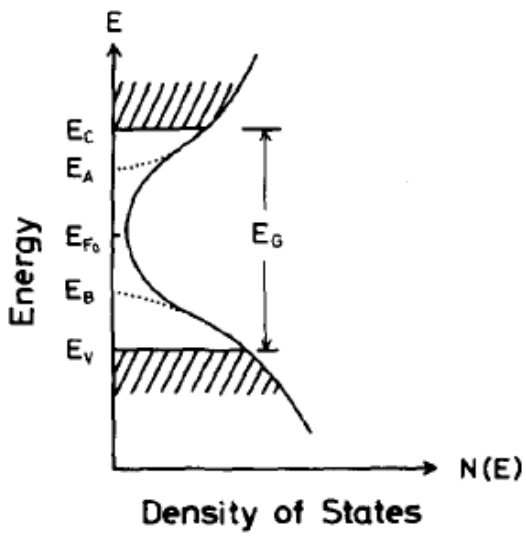


FIGURE 1: Electronic density of states for undoped polycrystalline silicon [15].

Several key papers have appeared over the years in support of the gap state structure of polycrystalline silicon and the origin of these states. For those with the time and inclination, highly useful background can be gleaned form [16] – [20].

The usual experimental result of a measurement of gap state densities is shown in Fig.2 [16]. Note both the exponential nature of the tailing states rising to the band edges and the actual density levels that such localized states can reach.

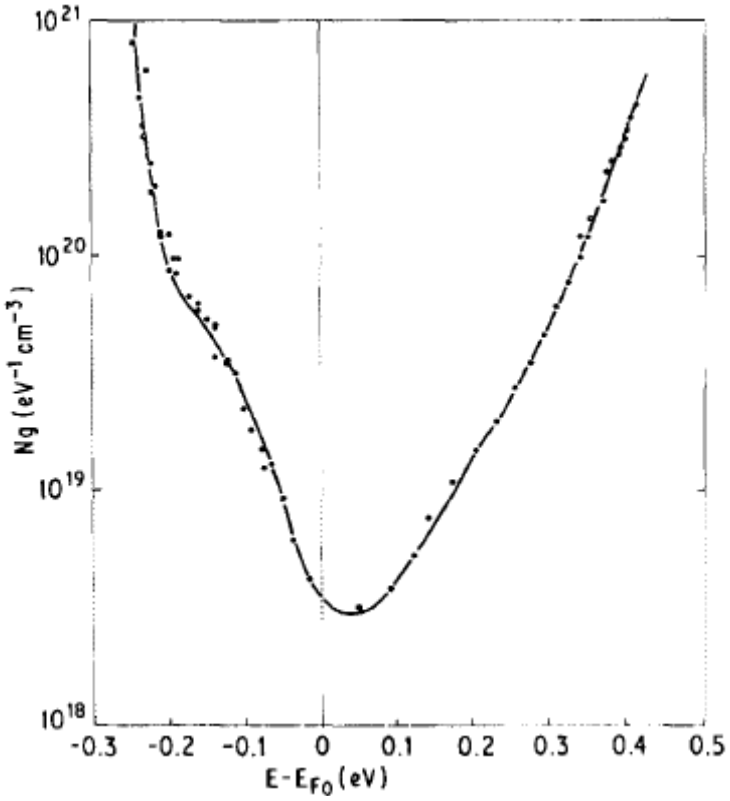


FIGURE 2: Density of states in the forbidden gap as measured using field effect transistors [16].

Having different grain sizes within the channel region can be seen as varying the levels of disorder. Intuitively, smaller grains introduce more disorder in the channel and should result in greater levels of localized states. This is a result that has been confirmed by many authors (see for instance [16]) and was studied by the author too [13]. Figure 3 shows the measured density of gap states for three different polycrystalline silicon thicknesses and grain sizes. TFTs with a channel thickness of 6 nm extinguished anomalous leakage effects

allowing barrier heights to be measured at very low gate – source voltages (and incidentally were the thinnest silicon channel TFTs made up to that time).

The next section looks at the effects of such levels of gap states on important field effect parameters such as the ability of the gate – source voltage to affect surface potential in the channel and the "energy deficit" from the conduction band edge.

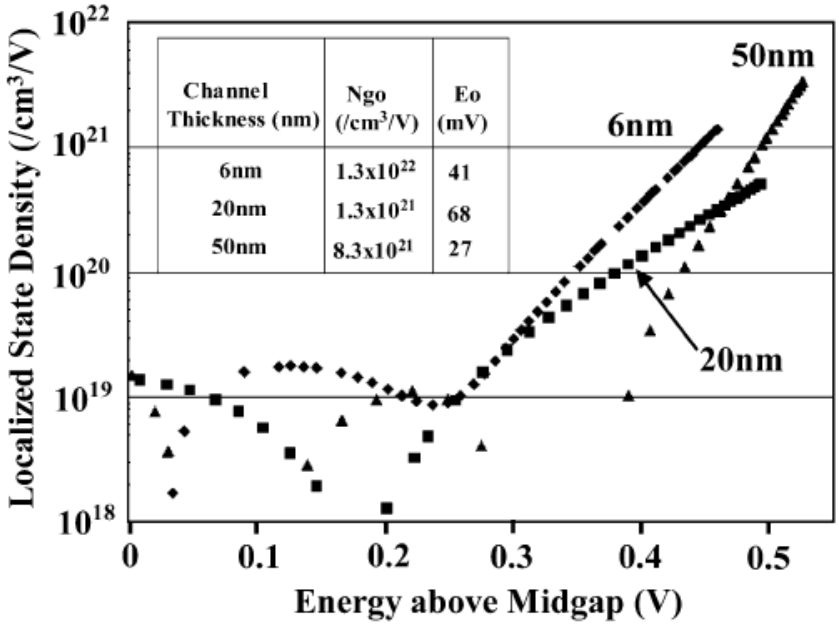


FIGURE 3: Localized state densities as a function of energy above mid-gap for three n-type TFTs with three different channel thicknesses. The original paper describes the parameters and method used [13].

III. The Surface Potential and Energy Barriers

In a MOS transistor with a monocrystalline channel, interface state density increases in magnitude as the energy approaches the band edges [21]. The interface states reduce the

ability of the gate voltage to create a given surface potential [22]. This is seen as a "stretchout" of the MOS capacitance – voltage curve and an increase in the inverse subthreshold swing of a MOS transistor (in mV/decade). The induced charge in the semiconductor channel region is made up of a mobile part and an immobile part where the latter is trapped in the interface states. For a given gate voltage, a transistor with a larger fraction of immobile trapped charge will need a larger voltage to induce the same amount of mobile charge compared to a transistor with a smaller fraction of immobile charge.

The effect of gap states in TFTs with polycrystalline channels is similar but of a much larger magnitude. The effect of the gate voltage on the surface potential is severely weakened by the large population of localized states to such an extent that the Fermi level never reaches the conduction band edge (n-type TFT but can be extended to p-type) within the operational voltages of the device. The resulting energy deficit (conduction band edge to Fermi level in channel) increases with increasing disorder in the channel.

Figure 4 shows the surface potential as a function of gate – source voltage as measured by the author on n-type TFTs with different channel polycrystalline silicon thicknesses and grain sizes (and therefore different disorder levels) along with a comparison with an NMOS transistor in the monocrystalline bulk which had a gate oxide thickness equivalent to the effective oxide thickness of the TFTs [13]. Several important points stand out. Firstly, notice the ease with which the gate controls the surface potential in the case of the monocrystalline channel. Not only does the conduction band edge reach the Fermi level but it does so within 1 volt. Secondly, in contrast, notice how the TFTs' surface potential is a much weaker function of gate – source voltage. Even after 5V on the TFT gate with respect

to the source, the conduction band edge is still "bogged down" below the Fermi level. The resultant energy deficit is greater for larger channel disorder.

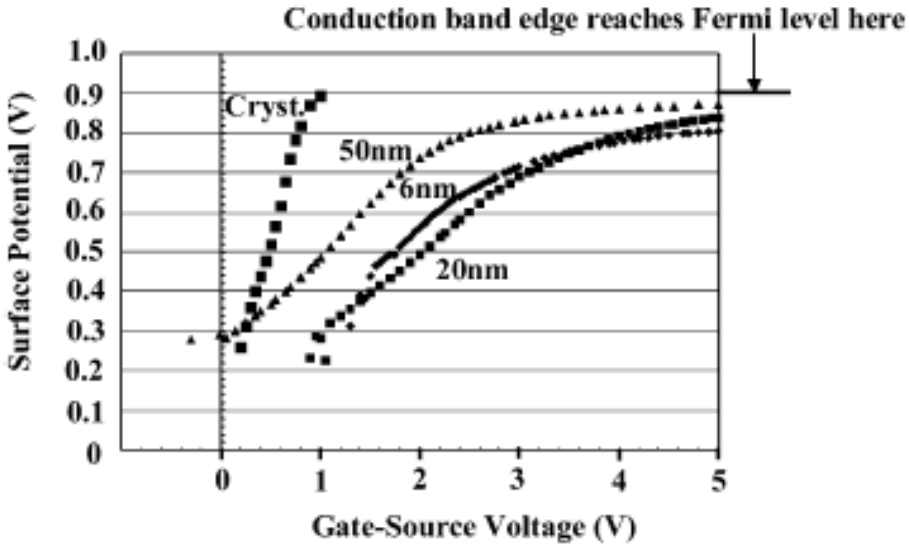


FIGURE 4: Surface potential as a function of gate – source voltage for monocrystalline NMOS and polycrystalline silicon nTFTs [13].

Another way to look at this is to plot the energy barrier to current flow from the source to drain as a function of gate – source voltage. Figure 5 shows this for the same devices as in Fig.4 [13]. A similar analysis has been published for both n-type and p-type TFTs [23]. This is the energy difference between the Fermi level and the conduction band edge in the n-type TFT at the channel surface. In other words, it is the energy barrier between the source and the inverting channel.

Figure 5 is perhaps the clearest of all the different ways of looking at the transistor conduction mechanism. In monocrystalline silicon transistors, the energy barrier at the source is quickly brought down to zero within a volt between the gate and source. This is

seen as a small inverse subthreshold swing in mV/decade. Disorder in the channel results in a "sluggish" energy barrier response to the gate – source voltage. Even after 5 volts on the gate with respect to the source, an energy barrier remains with its magnitude dependent on the level of disorder in the channel. The conduction band edge cannot reach the Fermi level within normal device voltages. The sluggishness of response only increases with gate – source voltage. The consequences are large inverse subthreshold slopes and small source – drain currents with the latter being temperature activated. A simple "back-of-the-envelope" calculation using an equivalent energy deficit of 0.1 volt results in about 2% of the mobile electron population in the inversion channel compared to the crystalline case with zero energy deficit. And all because of those localized states in the band gap.

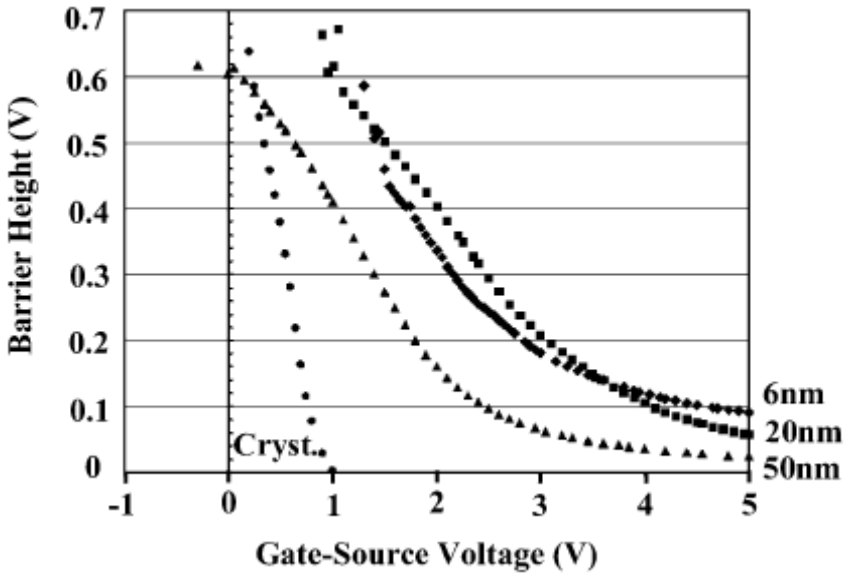


FIGURE 5: Energy barrier in volts for monocrystalline NMOS and nTFTs [13].

The next section applies these ideas to any NAND Flash string with polycrystalline channels.

IV. NAND Flash Strings with Polycrystalline Channels

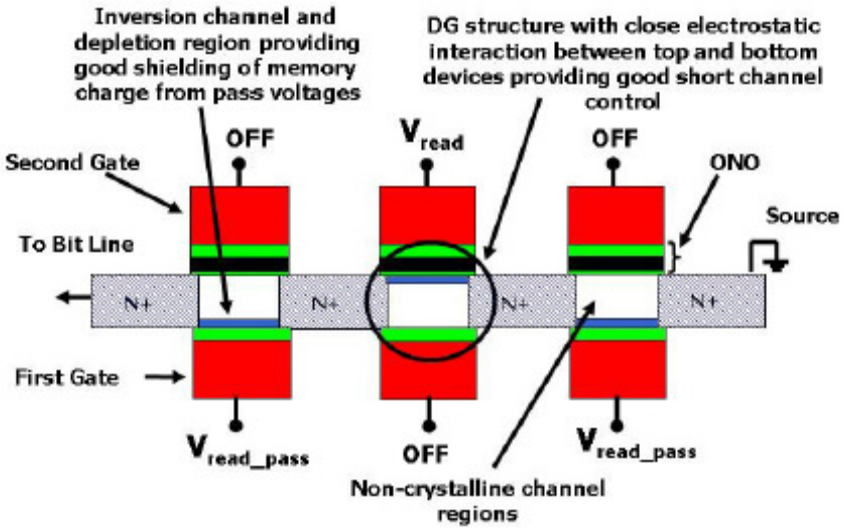
In NAND Flash, memory devices are placed in series strings. When reading one cell, all the other cells in the same string must conduct. The gate voltage on these “must-conduct” cells is called the read-pass voltage. The impedance of each of these must-conduct cells is dependent on its memory state. The low threshold voltage erased state has lower impedance than the high threshold voltage programmed state. The worst case (smallest) string current is defined when the cell being read is the only cell in the string that is in the erased state. All the other cells that must conduct are in the programmed state.

The above consideration for worst case string current is no different when applied to a NAND string consisting of a polycrystalline channel. However, the situation is much worse because of the small currents out of each cell. The effects of channel disorder have been described in Section III. Not only is the string current smaller in the case of a disordered channel, but also the difference between best case and worst case string current is accentuated. In addition, the ability of the gate voltage to increase the worst case string current is severely limited compared to the monocrystalline channel case.

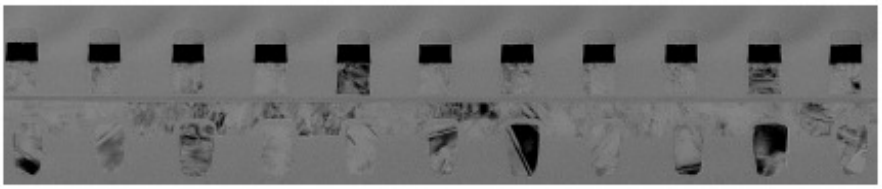
A previous paper introduced the effect of lengthening strings in vertically oriented 3-D NAND on the worst case string current [24]. Here, we generalize the approach for any NAND string with a polycrystalline channel. Manufacturers tend not to publish such worst case string currents for polycrystalline channels with the result that [24], [25] and [26] were the only places, as far as the author knows, where this was done.

As a recapitulation of the string measurement, Fig.6 shows the structure used. The Dual-Gate TFT SONOS string allows the memory cell being read to be accessed in a way that leads to natural electrical shielding of any stored charge and therefore close to zero pass

disturbs [25], [26]. To measure string currents in a fashion that mimics a NAND string, all the memory gates are turned off except the cell being read. All the non-memory gated devices are turned on with a gate voltage called the read pass voltage. The non-memory gated device opposite the memory cell being read is turned off. The current path is then from the bitline of the string through the inversion channels of the non-memory gated devices, through the memory cell being read and then through the rest of the non-memory gated devices to the grounded source of the string. The n-type source-drains link up the inversion channels. The threshold voltage of each access device is around 2 volts (at 10 nA source – drain current). Since this is fixed, we use the concept of the read pass overdrive voltage on these devices which is the voltage over and above this threshold voltage. This then generalizes the concept to any TFT NAND string with a polycrystalline channel where the important parameter for string current is the gate voltage on a passing memory cell over and above its highest programmed threshold voltage state.



(a)



(b)

FIGURE 6: The concept behind the DG-TFT-SONOS that allows the generalized measurement of the string current in any NAND string with a polycrystalline channel. (a) A schematic cross section of the string showing how a memory cell is read. (b) A Transmission Electron Micrograph cross section of an actual DG-TFT-SONOS string [25], [26].

Figure 7 is a reworking of the data given in [24] with the read pass overdrive voltage given on the X-axis.

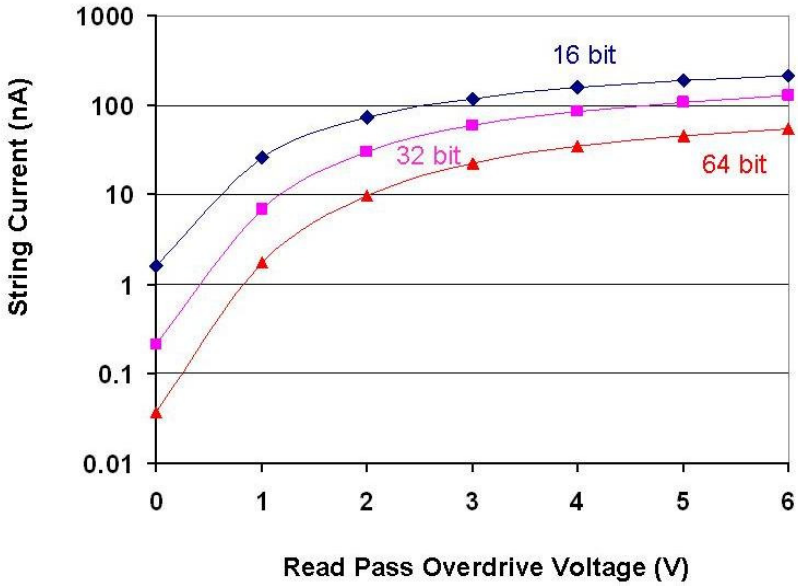


FIGURE 7: String currents with a polycrystalline channel measured as a function of read pass overdrive voltage for different string lengths. The structure is described in [24] – [26]. The electrical conditions are given in [24].

What Fig.7 shows is, for example, a 32 bit string with a threshold voltage window of about 5V would have a best case string current of around 100 nA with a 5V read pass overdrive voltage. The equivalent worst case string current, when all other cells are in the high threshold voltage programmed state and assuming a read pass overdrive voltage of 1 volt above this programmed state, would be less than 10 nA.

In the case of the 64 bit string, the best case string current with a 5V read pass overdrive voltage is about 50 nA. This then drops to about 1 nA for the worst case string current assuming a 1 volt overdrive of the programmed state threshold voltage.

An extrapolation can be made for a 128 bit string where the equivalent numbers would be about 15 nA and 0.5 nA for the best case and worst case string currents respectively.

A recent paper showed a value of around 100 nA for a 32 bit string with a read pass voltage of 7 volts [27]. The erased threshold voltage was about 1 volt while the programmed state was about 6 volts. Whether the 100 nA was best or worst case was not mentioned in the paper but a comparison with the data here suggests strongly that it was probably the latter. Having a read pass voltage of 7 volts with the programmed threshold voltage at 6 volts would give a 1 volt read pass overdrive voltage for the worst case condition. This would result in a value of around 10 nA or less for the worst case string current.

Figure 7 shows the weakness of the read pass overdrive voltage in trying to increase the string current. An additional challenge is the increasing read pass disturb for increasing read pass voltages. Figure 7 shows that a 1 volt increase in read pass overdrive voltage to 2 volts increases the worst case string current by several nA's. This would then come at the

expense of about a 2 decade decrease in read lifetime in an optimized charge trap dielectric stack [12].

Using the knowledge gained in Section III, we can understand the shape of the curves in Fig.7. Notice the similarity of the surface potential – gate voltage curves in Fig.4 with the string current – read pass overdrive voltage curves in Fig.7. The population of conducting electrons in the inversion channel is an exponential function of the surface potential [28]. The string current is directly proportional to the population of conduction electrons. Therefore, the logarithm of the string current should vary with gate voltage in a similar fashion to the surface potential variation with gate voltage as is the case.

The NAND string can be viewed as a single MOS transistor with incremental sections along the gate direction from source to drain each having a different threshold voltage. In the worst case for string current, all these sections except one have the high programmed threshold voltage. The read pass voltage on these sections is attempting to “drag down” the conduction band edge (in our n-type TFT case) towards the Fermi level. As we have seen in Section III, the disorder in the channel leads to large populations of gap states that seriously inhibit this band bending. Therefore, potential barriers remain inhibiting electron flow between the source and bitline.

It is instructive to compare the above experimental results with others. For instance, Kim et al. [14] show both experimental data and simulation results to test the effect of grain boundary traps within the channel of a TFT. Their experimental data showing the impact of large grains versus small grains in the channel is consistent with the author’s data in that the source – drain current is smaller and remains smaller within the operational voltage of the device in the small grained sample (their Fig.4). However, their simulations show that

increasing trap densities only lead to larger inverse subthreshold swings (in mV/decade) and that the reduced currents can be overcome completely at relatively small gate voltages (their Fig.5). This latter point is not consistent with their own data and with the data discussed above.

Figure 8 is a reworking of Fig.7 with Section III's learning added together with the critical points for the best case and worst case string currents. Note also the "educated guesses" for the even longer strings derived from the experimentally determined data. The best case is marked at a 5 volt read pass overdrive while the worst case is at 1 volt but the reader can move along the curves to see what happens at higher read pass overdrive voltages. These educated guesses are particularly appropriate to the vertical NAND Flash approaches known as BiCS and TCAT [1], [2], [3], [5], [6] since memory capacity increases are achieved through string lengthening.

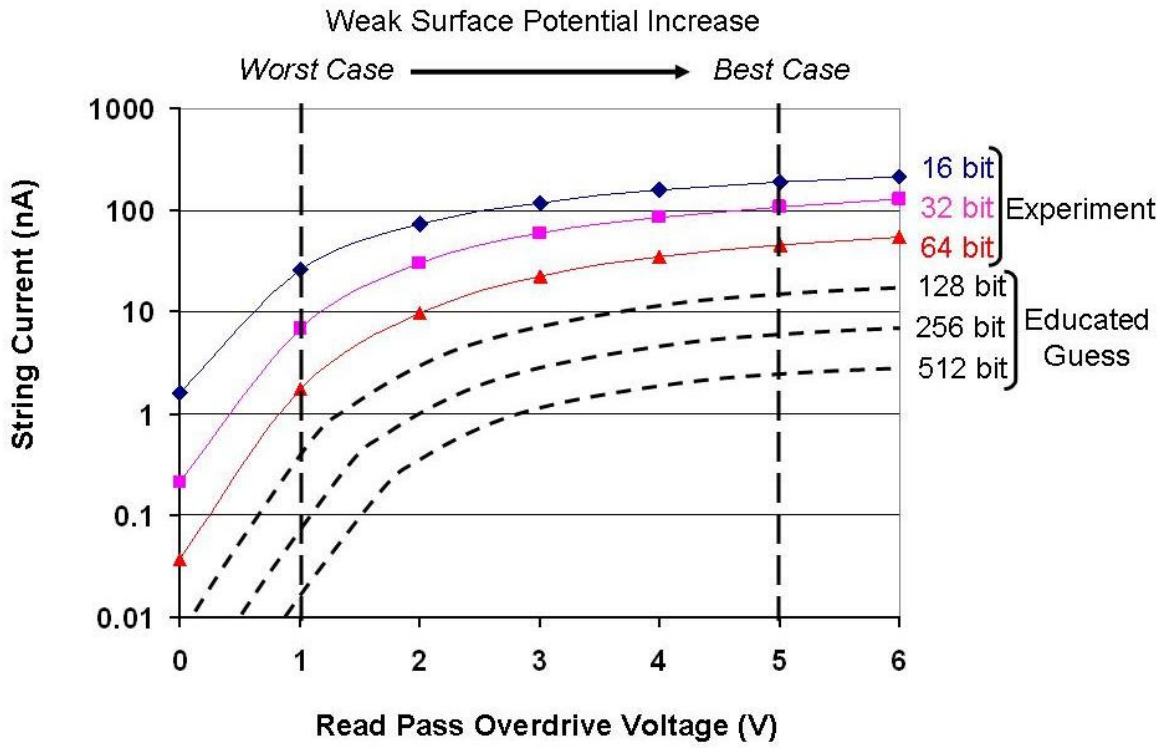


FIGURE 8: String currents with a polycrystalline channel measured as a function of read pass overdrive voltage for different string lengths as in Fig.7. The worst case and best case conditions are marked using a 1 volt and a 5 volt read pass overdrive condition respectively. "Educated guesses" for the longer strings are given.

Table 1 summarizes the worst case string currents as a function of string length and for several read pass overdrive voltages.

String Length (number of cells)	Worst Case String Current at 1 volt read pass overdrive (nA)	Worst Case String Current at 2 volt read pass overdrive (nA)	Worst Case String Current at 3 volt read pass overdrive (nA)
16	26	75	120
32	7	30	60
64	1.5	10	20
128	0.5	3	7
256	0.1	1	3
512	0.02	0.5	1

TABLE 1: Data and educated guesses for the worst case string current as a function of string length and read pass overdrive voltage. **Data in blue**, **educated guess in red**.

V. Summary and Conclusions

The disorder introduced into the channel of a 3-D NAND Flash string by the use of polycrystalline material has serious consequences for the level of current expected from the string. Using the concept of band gap localized states and their effect on the ability of the gate voltage to alter the surface potential, it has been shown that removal of energy barriers

to electron flow within the string channel cannot be achieved within the normal operating voltages of the device. The key points are:

- Worst case string currents drop below nA levels beyond 64 bit strings;
- Significant roll-off from best case to worst case string currents;
- Read pass voltages have very little effect on the worst case string currents;
- Read pass voltages will have a large effect on read pass disturb.

The vanishing worst case string currents should cast some doubt on the viability of the vertically oriented NAND Flash approaches referenced above. In addition, the roll-off from the best case to worst case string current in any NAND string with a polycrystalline channel should be noted.

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