The Erase Advantage in DG-TFT-SONOS 3-Dimensional Flash

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Abstract

The ability to erase the memory state in a thin-film transistor (TFT)-based Charge Trap Flash (CTF) cell is done in several ways depending on the process and device architecture. This paper explains the advantage that the Dual-Gate TFT SONOS (DG-TFT-SONOS) has over the other main 3-D TFT CTF approaches.

I. Introduction

Vertically oriented Charge Trap Flash (CTF) NAND such as Bit Cost Scalable (BiCS) has appeared as an apparently strong contender to replace classic 2-D NAND Flash [1], [2], [3], [4]. The main reason for such current popularity is the decreasing relative bit cost as the memory capacity increases through the stacking of more layers. The standard alternative approach for 3-D stacking of CTF NAND is given by the TANOS architecture [5].

In both approaches, special consideration needs to be paid to the erase method. In BiCS, erasing cells within the vertical NAND string requires the generation of electron-hole pairs

due to Gate Induced Drain Leakage (GIDL). This involves taking the gate of a string select transistor negative with respect to its junction. The high fields at the drain result in GIDL current generation such that holes get injected into the vertical channel of the string. This sets the potential of the channel of the string such that a negative potential can be applied to any control gate to erase any cell in the string.

GIDL itself requires large fields within the gate-drain overlap region of the select device [6]. These fields produce hot carriers that can lead to gate dielectric degradation [7], [8]. At the time of writing this article, some data have been published [4] showing BiCS endurance characteristics to 1000 program/erase cycles. However, the corresponding retention seems to be given only for a fresh uncycled device. The real test would be retention of cycled cells. Another interesting challenge may be the amount of current required to erase a full memory since GIDL could result in a sizable current per NAND string compared to the standard erase tunneling currents.

In the more standard NAND strings in 3-D, erasing a cell within a string would be a slow process if access to that cell was required through the other string cells [5]. To achieve fast erase in these cases, a special contact has been introduced, called the source-body tie. This shorts the p-type TFT body to the source with a special contact allowing erase to take place as in standard bulk NAND Flash. Besides the added process complication, other disadvantages of this approach include:

- the need for a thicker TFT body than otherwise would be needed leading to potential scaling problems;
- the inability to voltage bounce the source during programming thus resulting in increased program disturb;

It is with these considerations in mind that the Dual-Gate TFT SONOS (DG-TFT-SONOS) can be shown to have significant advantages during erase.

II. DG-TFT-SONOS

The fabrication sequence used to make the devices in this study has been reported elsewhere [9], [10]. As was shown, the channel of these devices is nanocrystalline silicon. A schematic cross section is given in Fig.1(a) for ease of understanding. Figure 1(b) shows a TEM cross section of the actual string.

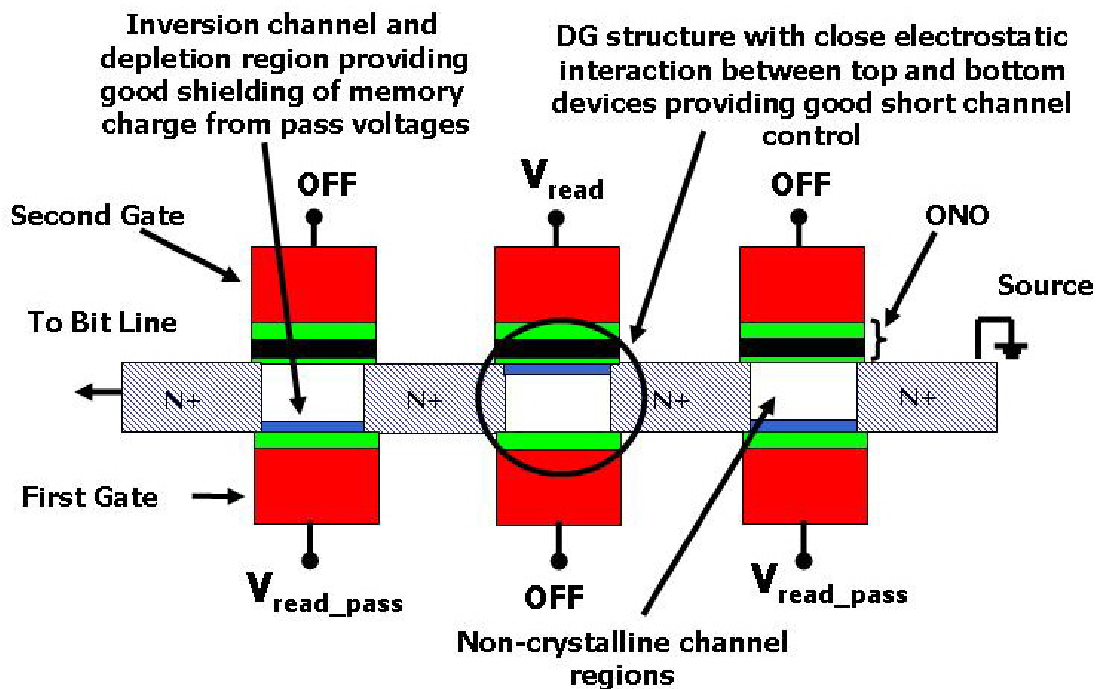

Figure 1(a): *The basic concept of the dual-gate series string Flash showing simultaneous shielding of stored charge during pass voltage application and intimate electrical interaction for good short channel control. Notice its ability to overdrive the non-memory gates to connect the memory device to the string ends. This overdrive has no disturb effect on the passing cells.*

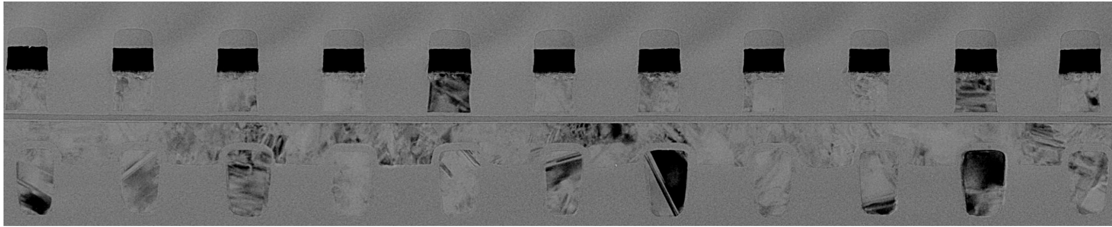

Figure 1(b): *Transmission Electron Micrograph of the structure with cut made parallel to the channel direction.*

The operation of the device has also been given in the literature [9], [10]. Here, the operation during erase is explained.

III. Erase

Figure 2 shows how erase is carried out in the DG-TFT-SONOS memory string.

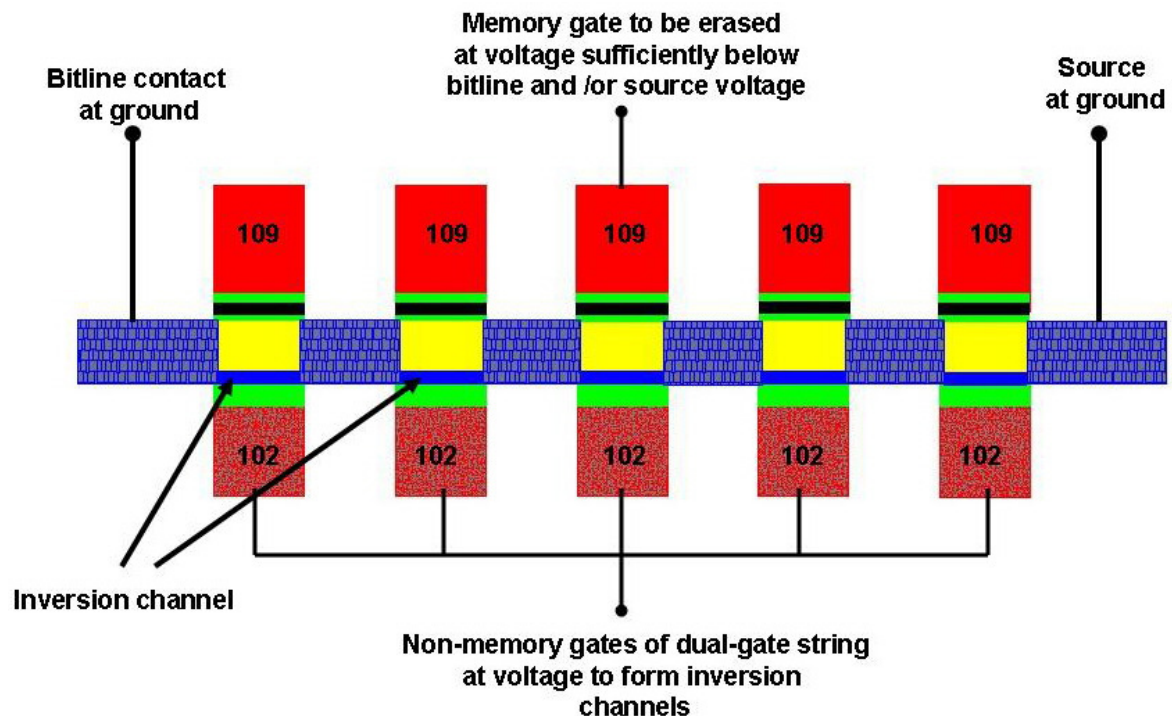

Figure 2: *Erase is carried out by using the non-memory gates to invert the channel material opposite to the memory devices. This then electrically links up all source-drain*

regions in the string. A voltage is then applied to the bitline contact and/or the source tying the isolated channel regions to within a diode of the bitline and or source voltage. Notice that the erase of any cell in the string is basically the same as the erase of a single cell not in a string.

The ability to use the non-memory gates to link up any source-drain and channel of any cell to the bitline and/or source allows a very flexible approach to erase that does not need a GIDL approach. A special source-body tie is also unnecessary.

Figure 3 shows the programming and erase endurance of the mid-cell of a 32 cell string of sub-50nm devices. No other second-gated memory devices are used in the cycling.

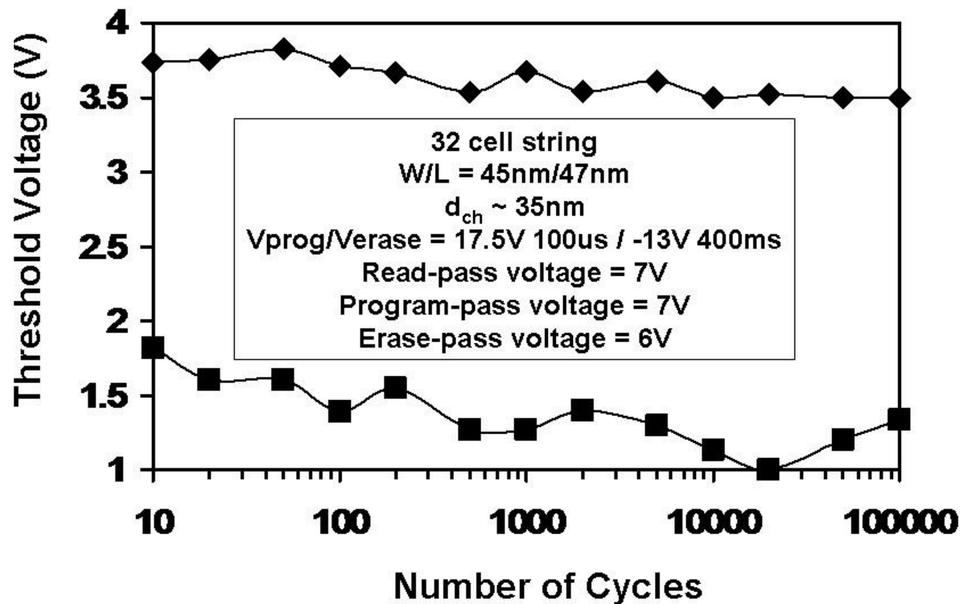

Figure 3: *Program/erase of a mid-cell in a 32 cell string using the method described.*

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IV. Conclusions

The DG-TFT-SONOS architecture allows flexibility in erase that avoids the use of GIDL and any special source-body tie. In this way, the conditions for the erase of a single cell can be extended easily to any length of memory string.

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