On Vertically Oriented Charge Trap NAND Flash as 3-D Memory

Andrew J. Walker

Schiltron Corporation

1638 Cornell Drive
Mountain View, CA 94040 USA
(email: andy@schiltron.com ; tel: +1 408 425 4150)

Abstract

Much has been reported recently on the cost advantages of various 3-D vertically oriented Charge Trap NAND Flash approaches as possible replacements for classic 2-D NAND Flash. What has been missing in the literature are data and discussion on the effects of such stacking approaches on the string currents expected to be sensed. For the first time, this paper shows that the combination of non-crystalline channels and ever-lengthening strings leads to quickly vanishing string currents such that these approaches have limited ability to replace classic 2-D NAND Flash.

I. Introduction

Vertically oriented Charge Trap Flash (CTF) NAND has appeared as an apparently strong contender to replace classic 2-D NAND Flash [1], [2], [3], [4], [5], [6]. The main reason for such current popularity is the decreasing relative bit cost as the memory capacity increases through the stacking of more layers. While this may not be in doubt, the fact that memory capacity increases are mainly achieved through NAND string lengthening should

lead to concern as to what happens to the string currents. The critical situation is when the memory cell being read is in the erased state while all other memory cells are in the high threshold voltage and therefore high impedance off state resulting in the worst case (i.e. smallest) string current. It is rather surprising that this concern has not been mentioned up until now especially since the channel regions of the reported devices are either amorphous or polycrystalline in nature so that currents in even the shortest string may be quite small compared to the 2-D crystalline version.

This paper presents an investigation into the effects of string lengthening carried out on deep submicron CTF series strings of dual-gate thin-film transistors having channels consisting of nanocrystalline silicon. Although not identical in physical structure to vertical gate-all-around CTF NAND strings, the unique structure allows worst case string currents to be measured in non-crystalline channels as a function of string length using different voltages to pass the current without any risk of disturbing these pass cells in the string [7], [8]. In this way, the pass voltage needed to maintain the string current at a certain level as string length increases can be easily determined without disturb clouding the issue. As will be seen, the worst case string currents in NAND strings with non-crystalline channels rapidly decline with string length. This is exacerbated for the vertical NAND strings already referenced by the fact that any increase in the pass voltage that could be used to maintain string currents is seriously limited by resulting disturbs.

II. Experimental

The fabrication sequence used to make the devices in this study has been reported elsewhere [7], [8]. As was shown, the channel of these devices is nanocrystalline silicon. A

schematic cross section is given in Fig.1(a) for ease of understanding. Figure 1(b) shows a TEM cross section of the actual string.

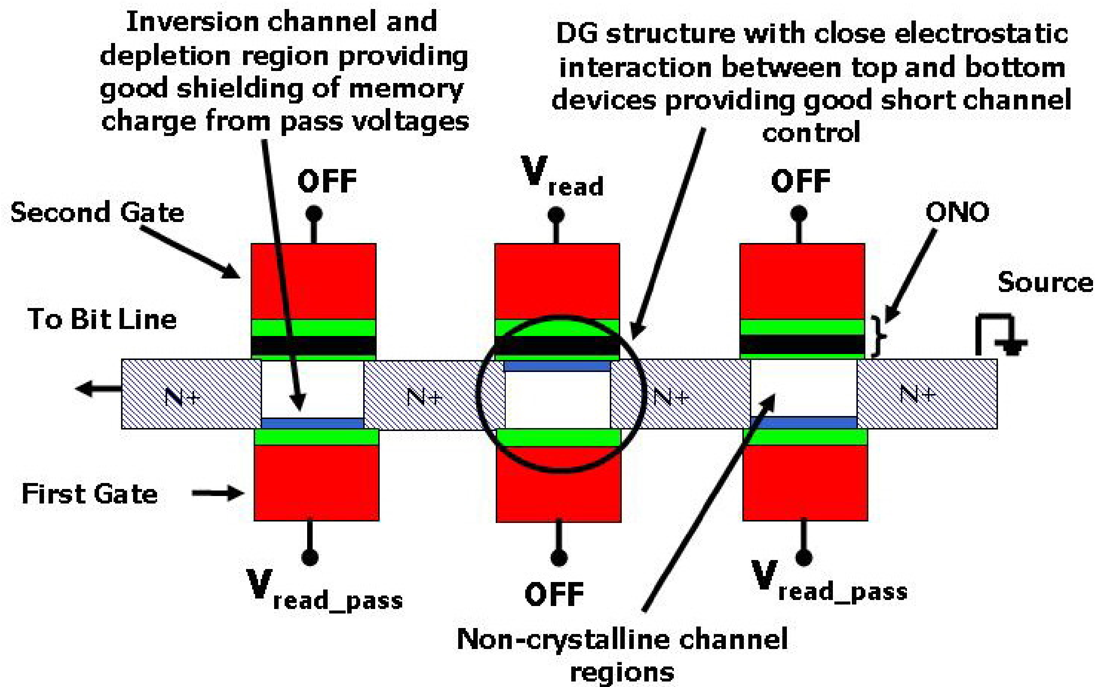

Figure 1(a): *The basic concept of the dual-gate series string Flash showing simultaneous shielding of stored charge during pass voltage application and intimate electrical interaction for good short channel control. Notice its ability to overdrive the non-memory gates to connect the memory device to the string ends. This overdrive has no disturb effect on the passing cells.*

Figure 1(b): *Transmission Electron Micrograph of the structure with cut made parallel to the channel direction.*

When a memory cell is read, all the other memory devices in the string can be placed in the non-conducting off state while the non-memory devices are placed in the conducting state with the read-pass voltage. The access device opposite the memory device being read is placed in the off state. In this way, the worst case string currents can be measured as a function of both the string length (number of cells in series) and the read-pass voltage. The string current results should mimic quite accurately the situation in any of the vertically oriented NAND CTF approaches referenced above.

III. Results and Discussion

Figure 2 shows the worst case string currents in 16 cell and 64 cell strings. The gate length and width of an individual cell is around 75nm. All memory devices except for the one being read are off along with the non-memory cell opposite the memory device. The read-pass voltage is 3V in both strings. Notice the collapse of the worst case string current from close to 30nA to around 2nA in the plateau region. From a device perspective it is also interesting to see how flat the plateau region actually is. This is characteristic of any NAND string and is similar in many respects to a simple MOSFET with high source and drain resistance [9].

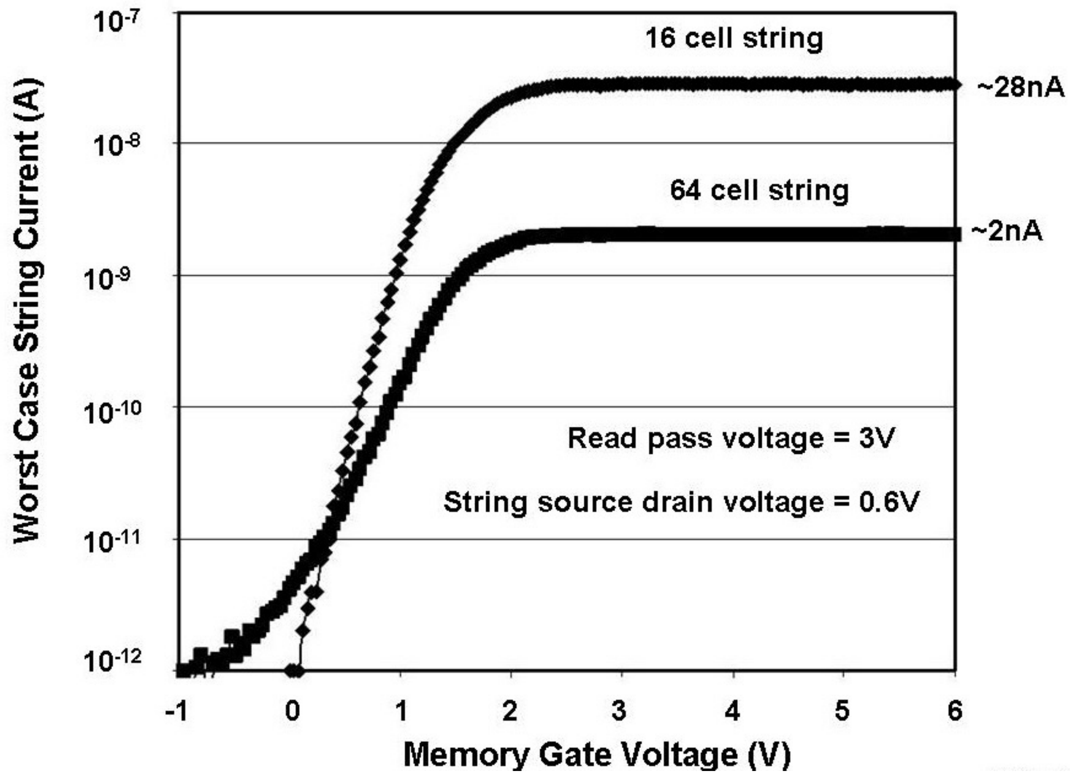

Figure 2: *The worst case string currents in 16 and 64 cell dual-gate strings. The memory cell's gate is swept while its opposite non-memory device is off. All other memory devices are off with -3V on their gates while their opposite access devices are turned on with a read pass voltage. In these cases, the read pass voltage was 3V, the string source to drain voltage was 0.6V and the non-memory gate opposite the device being read was at -3V. The lengthening of the string from 16 cells to 64 reduces the plateau string current from 28nA to 2nA.*

Figure 3 shows how the read-pass voltage can be used to lower the impedance of the connecting cells to the cell being read. Here, 8V was needed in the case of the 64 cell string to approach the worst case string current in the 16 cell string that used 4V read-pass voltage.

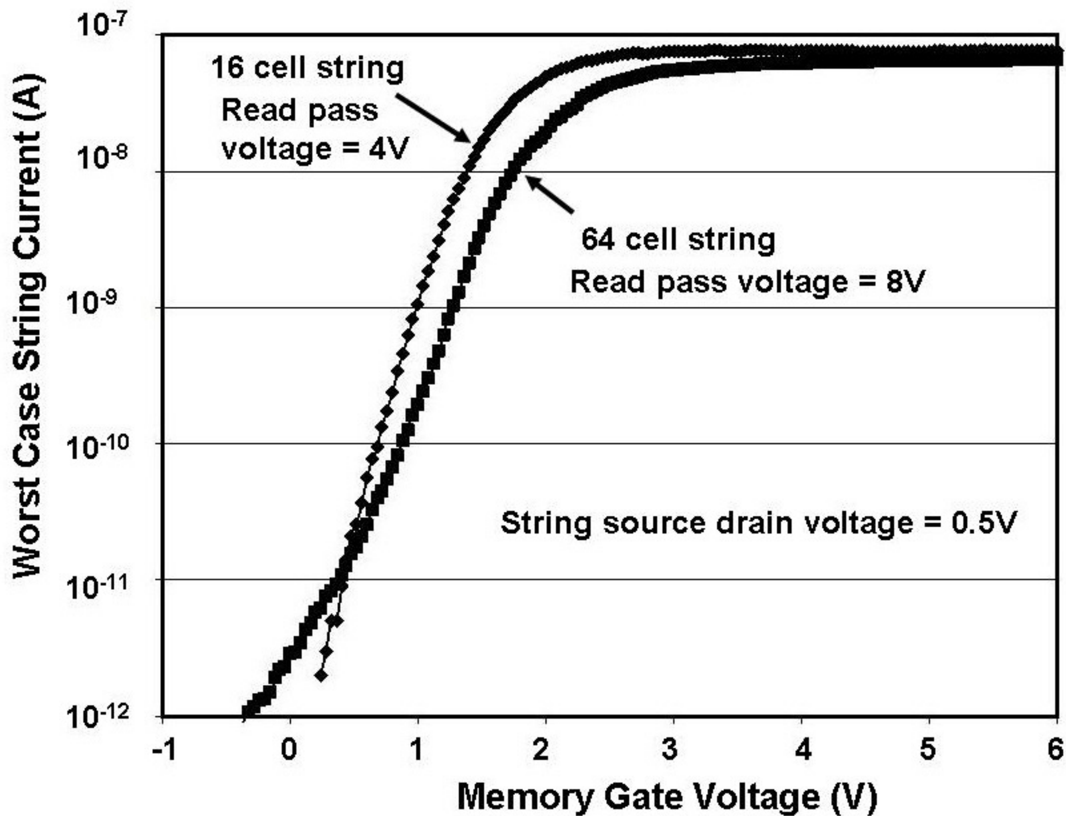

Figure 3: *The worst case string currents in 16 and 64 cell dual-gate strings and the effect of read pass voltage to try to sustain the string current. Again, the memory cell's gate is swept while its opposite non-memory device is off. All other memory devices are off with -3V on their gates while their opposite access devices are turned on with a read pass voltage. In these cases, the read pass voltage was 4V for the 16 cell string and 8V for the 64 cell string. The string source to drain voltage was 0.5V and the non-memory gate opposite the device being read was at -3V. If this measurement had been carried out on a classic NAND CTF string, the read pass voltages would cause a time dependent impedance in the string that would cloud the measurement.*

Figure 4 shows the worst case string current as a function of read pass voltage for various string lengths. Notice that an increasingly larger read pass voltage is needed to

sustain the worst case string current as the string is lengthened. For instance, to maintain 100nA as worst case string current, 4.6V pass voltage would be needed in the 16 cell string, 6.6V for the 32 cell string while apparently no amount of read pass voltage overdriving the gates would actually get to this current for the 64 cell string. The values for 50nA would be 3.5V, 4.7V and 7.4V respectively. Even if we assume that sensing capability improves with time and innovation, this falloff in worst case string current as non-crystalline channel CTF NAND strings lengthen is a major drawback in any of the vertical approaches referenced above.

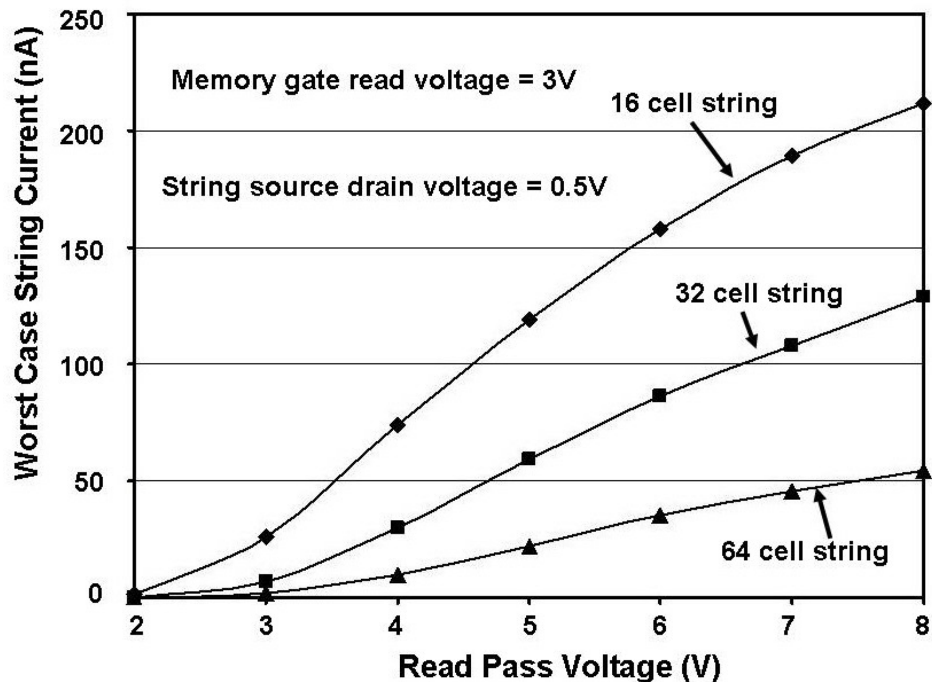

Figure 4: *The worst case string currents as a function of read pass voltage for the different string lengths. The memory device being read had 3V applied to its gate. The source to drain string voltage was 0.5V. All other memory devices were off with -3V on their gates along with the non-memory device opposite the device being read. Notice the collapse of the worst case string current as the string lengthens. Also, notice the ever increasing read pass voltages needed to sustain the string current as the string lengthens.*

The ability to use read pass voltage to compensate for this falloff is not a serious option in the case of these vertical string approaches since the resulting disturb of any erased state cell that experiences such an overdriving pass voltage will be extremely large [10]. In fact, the effect of such pass voltages is such that the time to shift the erased state threshold voltage by a certain amount varies exponentially with the inverse of the read pass voltage [11]. Clearly, gate dielectric optimization can be used somewhat to ameliorate this effect but even with optimized stacks the read pass disturb is extremely serious [11]. Also, such stack thickening towards 20nm [11] limits the lateral half pitch of any vertical CTF NAND string to greater than about 50nm since space is also needed for the gate and channel materials.

IV. Conclusions

The vertical CTF NAND string approach is certainly attractive from a cost point of view. However, the surprising lack of any information regarding the consequences on worst case string currents has now been removed. What this paper shows is that such approaches have quickly vanishing string currents as density is increased. The ability to use read pass voltages to sustain worst case string currents is severely limited by disturb considerations. Any gate dielectric stack optimization to ameliorate this effect is limited by lateral space considerations. Any further developments in these vertical CTF NAND strings need to comprehend these limitations.

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